LeCroy

WHITE PAPER

Physical Layer Testing of PCI Express and Other Serial Data Signals Using Consecutive Bits

Introduction

Traditionally, serial data signals such as Fibrechannel and Infiniband have used recovered clocks in their receiver circuits to detect the incoming data bits. More recent detection schemes use clock-less over sampling techniques in which the receiver compares bits sampled at several times the bit rate. The bits from each phase of the over sampled signal are then polled to determine the correct bit values. The development of the serial ATA standard and now PCI-Express, account for these different detection schemes through specification of the use of consecutive UI in the measurement of both eye patterns and jitter. Additionally, these interfaces employ spread spectrum clocking (SSC) in which the bit rate is slowly varied from its nominal value to .5% lower at a rate near 30kHz. The combination of the slow clock spreading with the need to measure consecutive bits gives rise to the need to measure thousands and even millions of consecutive bits in order to accurately characterize these physical layer signals. In addition, the interaction between specific bit patterns and the SSC clock can cause deviations in the peak jitter which can only be reliably captured using very long sequences of continuous bits. The method presented here uses a long real-time capture of bits along with a numerical clock recovery system to accurately measure both the eye pattern and jitter characteristics of serial ATA and PCI-Express signals in the presence of spread spectrum clocking.

Clock recovery

In order to measure the timing over a long sequence of consecutive bits, a local estimate of the bit rate must be made on segments of the data stream. This recovered clock must use the longest segment of bits over which the bit rate is reasonably constant. Spread spectrum clocking, for example, typically modulates the data at a 30KHz rate with a .5% peak deviation. The data rate estimate must be made over an interval short enough that the combination of the data jitter and peak SSC deviation are relatively small. This window is moved along the waveform in order to provide a clock estimate that is accurate for the bits being measured even when SSC is enabled. Clock recovery can be implemented using a numerical phase locked loop (see Figure 1).

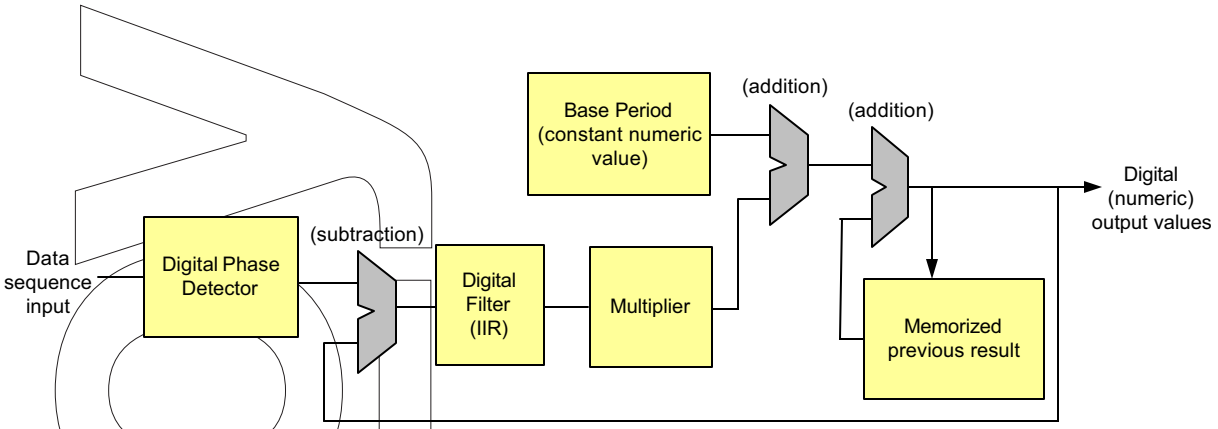

Figure 1 Flow Diagram of Numerical PLL

The output of the nume rical phase locked loop is a sequence of time values representing the transitions of a recovered clock. The base period of the data stream is the nominal bit rate and is selected by the user as a parameter. This period can also be computed from the data stream. The time value output from the PLL is computed by adding the previous value to the base period modified by a scaled and filtered version of the timing error between the previous time value and the current data edge. The IIR filter is implemented using a single parameter a which sets the weighting factor for previous periods in the correction factor. The filtered error values are described by the following equation:

$$\Delta t'_i = \Delta t'_{i-1}(1-\alpha) + \alpha \Delta t_i$$

This is the equation for a single-pole digital low-pass filter whose cutoff frequency is $2\pi\alpha$. Since the PLL updates at the data rate, the digital frequency is scaled to this rate. This gives a filter bandwidth of $F_d\alpha$. Where F_d is the nominal data rate. The current correction value is computed from a weighted average of the previous N values. The value of N can be viewed in terms of the weighting factor α as the point where $(1-\alpha)^N$ drops to 10%. For α equal to 1/1310, for example, this value is 3000 consecutive bits. An equivalent length of 250 bits can be approximated by an α value of 1/110.

Measuring Jitter and TIE

The timing jitter is defined for data streams as the time interval error (TIE). This parameter is the difference between the zero crossing times of the bits in the data stream and those of a reference clock. Each edge in the data stream is compared with the corresponding zero crossing of the reference clock which, for this measurement, is the numerical PLL described in the previous section. A sequence of time interval measurements is made, one for each edge in the data stream under test. Periodic jitter can be viewed by taking the Fourier transform of this sequence. The histogram of the TIE measurements gives an estimate of the PDF (Probability Distribution Function) of the TIE amplitude. The range of this histogram is proportional to the number of measurements of TIE contained in the distribution (more measurements increases the likelihood of measuring the more rare extreme values of the underlying distribution).

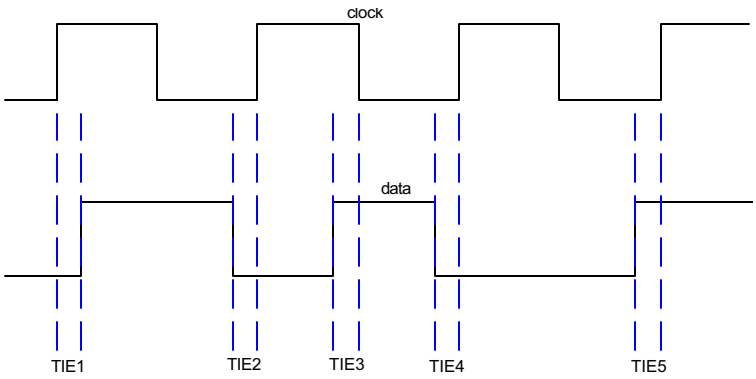

Figure 2 TIE measurement on consecutive bits

There are several techniques for evaluating the jitter from the TIE histogram. One can simply measure the standard deviation and range of the histogram or, as is the case with many standards, extrapolate the histogram for a more complete estimate of the PDF of the jitter and decompose this to its random and deterministic components. In the case of PCI-Express, a different approach is taken. The median (i.e. the histogram value with an equal number of population points above and below) and the maximum deviation from the median are used to determine the peak jitter. The jitter histogram is defined for any 250 consecutive bits (or data edges). The short record of 250UI allows measurements to be made with spread spectrum clocking enabled because the frequency estimate over this interval is reasonably constant. Applying the software PLL described above allows the measurement of this histogram over many thousands of UI. Such long records guarantee the capture of several cycles of the SSC modulation.

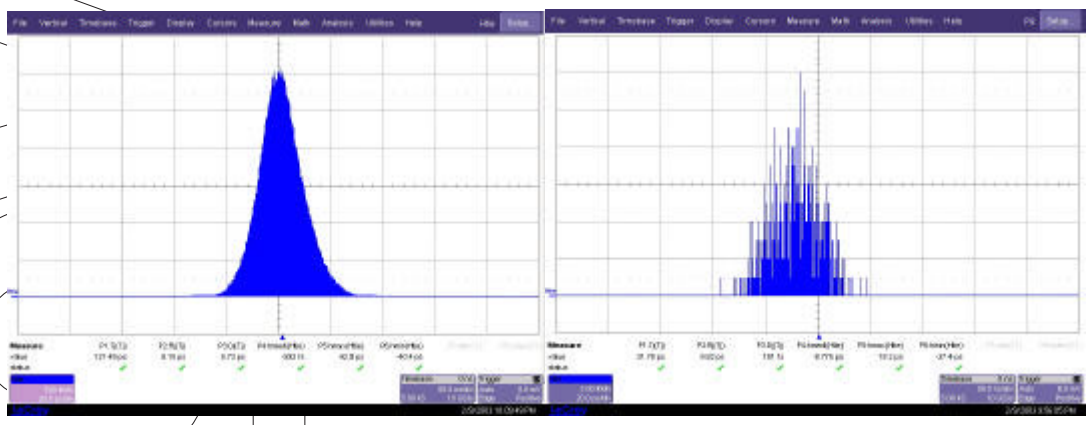

Figure 3 Jitter histogram: 300K bits using software PLL (left) and 250 bits using fixed frequency estimate

Histogram on the left is measured over 300K UI using a software PLL to generate a tracking reference clock. The image on the right is taken over 250 UI and using a fixed data rate estimate. While both histograms give accurate measurements of the range of jitter values, the one estimated over the longer data set is statistically more significant while at the same time including the time interva l error from every UI in the data set. The longer data set composed of consecutive UI also allows very accurate extrapolation of the jitter PDF giving the ability to extract random and deterministic jitter as well as total jitter for an equivalent bit error rate of 10^{-12}.

Eye Pattern Measurement

Eye patterns in the PCI-Express standard are measured on consecutive bits also. The algorithm consists of "slicing" the bit stream into bit-sized segments and overlaying the segments. This actually uses the same data set as the jitter measurement. The reference for slicing up the waveform is derived from the digital PLL described above. The transition times of the PLL are used to define the duration of each bit in the waveform. Since the period of the software PLL tracks low rate jitter, this has the desired affect of removing this jitter from the eye pattern. Figure 4 shows the eye pattern measured with and without the PLL enabled.

The eye patterns in Figure 4 are measured over approximately 300K bit periods or UI. It is clear that the PLL is necessary in order to give equivalent results to measurements over 250 UI as shown in Figure 5. The advantage of using a long record, however, is that all groups of 250 bits are included in the measurement.

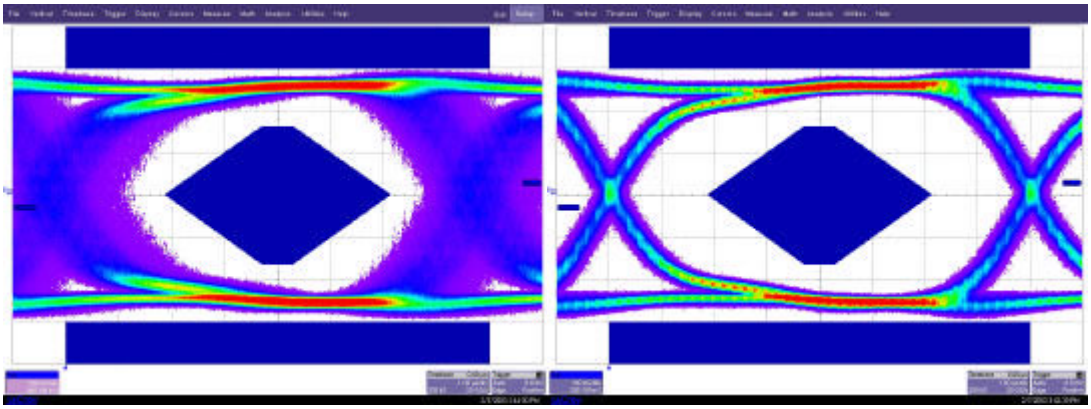

Figure 4 Eye pattern measurement with and without software PLL

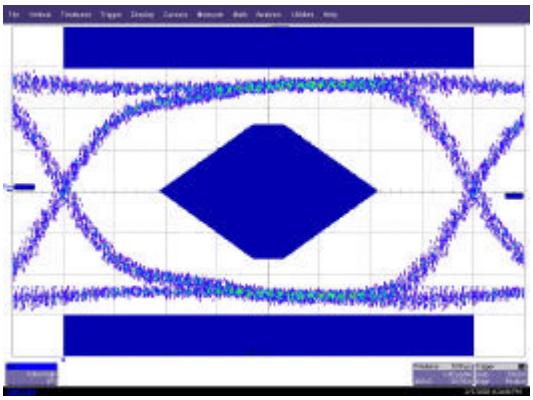

Figure 5 Eye pattern measured over 250UI

A particularly difficult problem is measuring eye patterns and jitter in the presence of spread spectrum clocking (SSC). While measuring the eye pattern over a relatively short record such as 250 bits will give accurate results, using a longer data set will give a complete measurement of the eye pattern for all SSC offset frequencies. Figure 6 shows an eye pattern measured using a 300K UI record using the software PLL and the same eye pattern measured using a short 250 UI record and a fixed data rate estimate. Again, we get similar results but over a much larger number of bits. The measurement with the software PLL, however, is capable of capturing any short term variations in jitter on the order of a few bits.

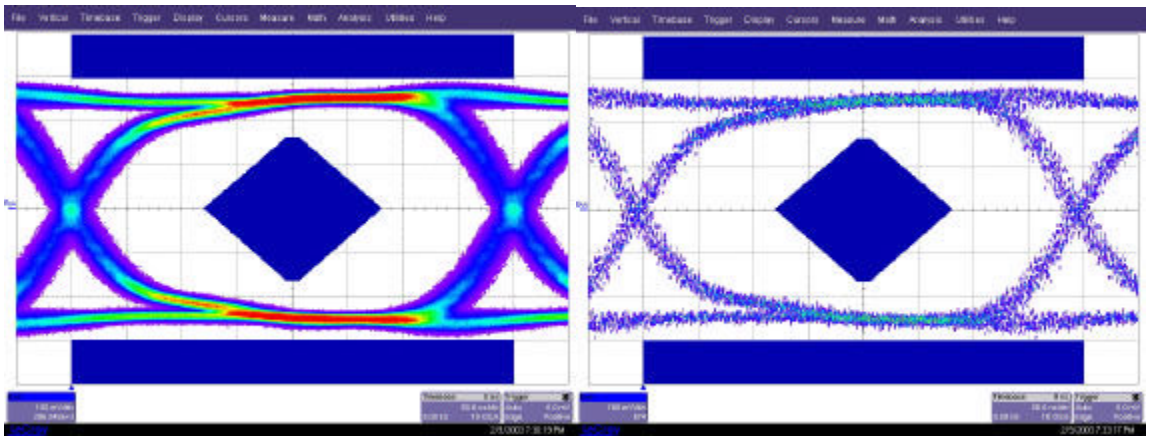

Figure 6 Eye patterns with SSC enabled. 300K UI with PLL (left) and 250UI without PLL

Conclusion

The development of over sampling detectors has created the need to measure consecutive bits in both jitter and eye pattern tests. While random sampling of data edges is a valid approach for evaluating performance of PLL-based detectors, it provides no information about the performance over consecutive bits. The current approach to testing uses relatively short sequences of consecutive bits and, while this is more than adequate under constant bit rate operation, spread spectrum clocking represents a difficult challenge. The combination of capturing long records of consecutive bits with configurable software clock recovery overcomes the limitations of both random sampling and short record capture giving accurate results for all operating modes.